## ABSTRACT OF THE DISCLOSURE

Disclosed is a semiconductor integrated circuit device having a mechanism of compensating not only circuit operational speed but also variations in leakage current, which includes: a main circuit constructed by a CMOS; a delay monitor 11 for simulating a critical path of the main circuit constructed by a CMOS and monitoring a delay of the path; a PN Vt balance compensation circuit 13 for detecting a threshold voltage difference between a PMOS transistor and an NMOS transistor; and a well bias generating circuit 25 for receiving outputs of the delay monitor 11 and the PN Vt balance compensation circuit 15 and applying a well bias to the delay monitor 11 and the main circuit so as to compensate the operation speed of the delay monitor 11 to a desired speed and reduce a threshold voltage difference between the PMOS and NMOS transistors.